

REMARKS/ARGUMENTS

Claims 1-49 are pending. Claims 1 and 3 have been rejected. Claims 2 and 4 have been objected to. Claims 5-47 have been allowed. Claims 1, 3, 5-6, 8-10, 15-18, 21-23, 25, 29, 35-36, and 42 have been amended. Claims 48-49 have been added. Reconsideration is respectfully requested.

The acceptance of the drawings is noted with appreciation.

Claims 1 and 3 have been rejected under 35 USC §102(e) as being anticipated by *Guenot et al.* (US Patent No. 6,529,026).

Claim 1 has been amended to recite in pertinent part “a high impedance control circuit including a single signal input coupled to a drain of said second MOS transistor and including an output coupled to a gate of said second MOS transistor.” Figure 2 of *Guenot et al.* has been cited as the basis of the rejection. However, Applicant notes that the reference numbers referenced in the Office Action refer to Figures 1 and 3. It is asserted that the operational amplifier 12 is a high impedance control circuit as recited in claim 1. Claim 1 has been amended to clarify that the high impedance control circuit includes a single signal input coupled to a drain of the second MOS transistor. In contrast, the operational amplifier 12 has two inputs, which are coupled to the drains of the PMOS transistor 6A and 6B. Instead, claim 1 recites that the single signal input of the high impedance control circuit is coupled to the drain of the second MOS transistor.

Lacking at least this claim feature, *Guenot et al.* cannot render claim 1 unpatentable. Because claim 2 depends on claim 1, for similar reasons *Guenot et al.* cannot render claim 2 unpatentable. Therefore, it is respectfully submitted that claims 1-2 are patentable over the references of record.

Claim 3 has been amended to recite in pertinent part “a high impedance voltage shifter including a single signal input coupled to a drain of said second MOS transistor and including an output coupled to a gate of said second MOS transistor.” It is asserted that the operational amplifier 12 of *Guenot et al.* is a high impedance voltage shifter as recited in claim 3. Claim 3 has been amended to clarify that the high impedance voltage shifter includes a single signal input coupled to a drain of the second MOS transistor. In contrast, the operational amplifier 12 of

Guenot et al. has two inputs, which are coupled to the drains of the PMOS transistor 6A and 6B. Instead, claim 3 recites that the single signal input of the high impedance voltage shifter is coupled to the drain of the second MOS transistor.

Lacking at least this claim feature, *Guenot et al.* cannot render claim 3 unpatentable. Because claim 4 depends on claim 3, for similar reasons *Guenot et al.* cannot render claim 4 unpatentable. Therefore, it is respectfully submitted that claims 3-4 are patentable over the references of record.

Claim 2 and 4 have been objected to as being dependent upon a rejected base claim that would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. New claims 48 and 49 include the subject matter of claims 2 and 4, respectively, as originally filed. Therefore, it is respectfully submitted that new claims 48-49 are allowable for the reasons that original claims 2 and 4 are allowable.

Claims 5-7 have been indicated to be allowable over the prior art of reference. Claims 5-6, 8-10, 15-18, 21-23, 25, 29, 35-36, and 42 have been amended to correct typographical or grammatical errors. No new matter has been added. It is respectfully submitted that claims 5-47 remain allowable.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 07-1896, **referencing docket number 2102397-992930.**

Respectfully submitted,

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